V-Band Amplifier Using InGaP/InGaAs/GaAs Heterostructure MESFET's with Asymmetric Au Gate Head

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***Abstract*— Self-aligned n^+ i-InGaP/n-InGaAs/i-GaAs heterostructure MESFET's (H-MESFET's) with a gate length of 0.16 μm were developed for applications to microwave and millimeter-wave wireless communication systems. A T-shaped Au/WSiN gate was used and the 0.8-μm-wide Au gate head was deliberately shifted toward the source in order to reduce the parasitic feedback capacitance. Shifting the Au gate head by 0.2 μm, the gate-to-drain capacitance decreased by 43 fF/mm and the maximum stable gain was improved by 1 dB. V-band monolithic microwave integrated circuit (MMIC) amplifiers fabricated with the asymmetric gate head field-effect transistors (FET's) achieved a gain of 9.7 dB at 55 GHz; their chip size is only 0.95 $\times$ 0.85 mm^2.**

I. Introduction

PLANAR structure GaAs MESFET's are superior to high electron mobility transistors (HEMT's) in terms of uniformity and reproducibility due to their simple and mature process. They appear to be the best candidate for highly integrated monolithic microwave integrated circuits (MMIC's) and mixed analog-digital IC's. We have developed subquarter-micron GaAs MESFET's and recently replaced ion-implanted channels with an InGaAs epitaxial versions due to its capability of forming a thinner layer with higher carrier concentration [1]. Moreover, we have employed a T-shaped Au/WSiN gate with large-volume Au head to reduce gate resistance. The large-volume Au gate head, however, results in higher parasitic gate capacitance as well as lower gate resistance. The influence of parasitic gate capacitance on FET performance becomes noticeable in the deep-submicron region since the intrinsic gate capacitance reduces linearly with gate length. In particular, the overhang of the Au gate head on the drain side significantly contributes to parasitic feedback capacitance which degrades FET amplifier gain.

In order to reduce the feedback capacitance, we have deliberately shifted the Au gate head toward the source. This letter discusses the relation between the movement of the Au gate head and a gate-to-drain capacitance, and shows the improvement in device gain possible with an asymmetric Au gate head. It also describes the design and the measured performance of the V-band MMIC amplifier by using cascode-connected FET's with an asymmetric gate head.

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II. Asymmetric Au Gate Head Structure

A schematic of an i-InGaP/n-InGaAs/i-GaAs heterostructure MESFET (H-MESFET) with an asymmetric Au gate head shown in the inset of Fig. 1. The detailed fabrication process of the H-MESFET is described in [2] and [3]. The epitaxial layer structure is 5-nm undoped GaAs/10-nm undoped $In_{0.48}Ga_{0.52}P$/12-nm Si-doped $In_{0.20}Ga_{0.80}As$/10-nm undoped GaAs on 3-in-diameter GaAs substrate [4]. The carrier concentration of the InGaAs channel was kept as high as 5×10^{18} cm^{-3} after rapid thermal annealing. It is also attractive to use InGaP as a barrier layer, because it increases the Schottky barrier height and suppresses gate leakage current [5]. All doped layers except a channel layer were formed by ion-implantation. n^+ and n' layers were formed self-aligned to the gate electrode by using 80- and 40-keV Si implantation with doses of 7.9×10^{13} cm^{-2} and 4.0×10^{13} cm^{-2}, respectively. The offset between the gate and the n^+-region was set to 0.25 μm. Bp and Bp2 layers were formed by using 50- and 90-keV Be implantation with a dose of 2.0×10^{12} cm^{-2}, respectively. Isolation was done by using 40-keV Oxygen implantation with a dose of 1.0×10^{14} cm^{-2}. The channel layer was passivated with 550-nm SiO_2 and 2.5-μm polyimide.

The device features symmetric BP-LDD (buried p-layer and lightly doped drain) structure and the spacing between the gate Schottky electrode and the source (L_{gs}) or drain Ohmic electrode (L_{gd}) is 0.9 μm. The gate length of refractory metal WSiN is as short as 0.16 μm and its height is 200 nm. A Au gate head with a width of 0.8 μm and a thickness of 1 μm was formed on the WSiN gate electrode by means of low-current gold electroplating [6]. The overhang of the large-volume Au gate head causes the parasitic capacitance. The gate-to-drain capacitance (C_{gd}) has especially an influence on FET gain performance as a feedback capacitance. C_{gd} is usually less than one-fifth or one-tenth the gate-to-source capacitance (C_{gs}). Hence, it is effective to shift the Au gate head toward the source. The movement of the Au gate head

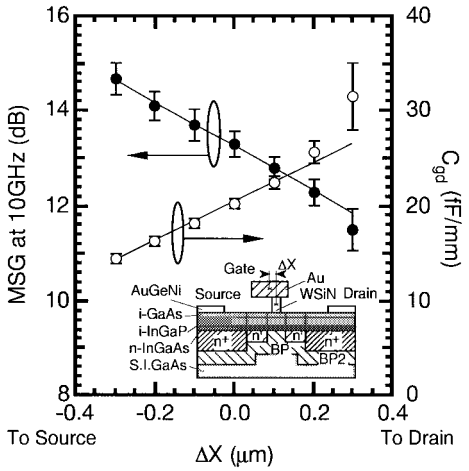

Fig. 1. Gate-to-drain capacitance and maximum stable gain at 10 GHz versus deviation of Au gate head from center position (ΔX). Inset is schematic cross-sectional view of InGaP/InGaAs/GaAs H-MESFET with asymmetric Au gate head.

away from the center (ΔX) was made due to an alignment of i-line photolithography with an accuracy of 0.05 μm.

III. Effect of Asymmetric Gate Head

The H-MESFET's with different ΔX were fabricated on the same wafer. The devices exhibited a transconductance (g_m) of 400 mS/mm with a threshold voltage ($V_{\rm th}$) of -0.3 V. The full channel current is 280 mA/mm. The gate-to-drain breakdown voltage is 4.5 V, defined at a gate leakage current of 50 μA/mm.

Fig. 1 shows $C_{\rm gd}$ and MSG (maximum stable gain) at 10 GHz versus the deviation ΔX. They are the mean values of 21 devices cross the wafer and the error bars are the standard deviations. $C_{\rm gd}$ and MSG were calculated from the S-parameters corresponding to fabricated devices with each ΔX. The gate width of the fabricated devices is 100 μm. The applied voltages were $V_{\rm gs} = 0.55$ V and $V_{\rm ds} = 1.5$ V. A minus value of ΔX represents shift toward the source and a plus toward the drain. $C_{\rm gd}$ was simply estimated from the imaginary part of the intrinsic Y-parameters, which were calculated by converting the measured S-parameters of the devices into Y-parameters and subtracting the Y-parameters of an open pattern to remove pad capacitance. In Fig. 1, $C_{\rm gd}$ linearly increases as ΔX increase at ΔX values below 0.2 μm: 21 fF/mm per 0.1-μm shift of the Au gate head, while MSG decreases as ΔX increase: 0.48 dB per 0.1-μm. The gap between the overhang of Au gate head and the channel is filled with SiO_2 by means of plasma enhanced chemical vapor deposition (PECVD). The capacitance between the overhang and the channel can simply be estimated to 19.0 fF/mm per 0.1-μm shift, where the dielectric constant of PECVD-SiO_2 is 4.3 and the gap is 200 nm. In this linear region, the increase in $C_{\rm gd}$ is mainly attributed to the capacitance between the overhang and the channel. Subsequently, a sudden increase of $C_{\rm gd}$ can be seen at ΔX values above 0.2 μm, because the parasitic capacitance between the gate overhang and the drain ohmic contact abruptly increases. It is possible to reduce this parasitic capacitance by widening the gate–drain spacing in case of asymmetric structure. The gate head shifting toward the source is more effective to reduce $C_{\rm gd}$, however, than the widening of gate–drain spacing, because the capacitance between the overhang and the channel can be decreased by the gate head shifts.

TABLE I
Equivalent Circuit Parameter of InGaP/InGaAs/GaAs H-MESFET. W_g Is 100 μm. ΔX Is -0.2 μm. Applied Voltages Were $V_{\rm gs} = 0.55$ V and $V_{\rm ds} = 1.5$ V

g_m (mS)	τ (psec)	R_i (Ω)	R_{gs} (kΩ)	R_{ds} (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)
55.0	0.2	1.1	4.3	163.0	97.1	16.2	30.0
R_g (Ω)	R_s (Ω)	R_d (Ω)	L_g (pH)	L_s (pH)	L_d (pH)		
2.0	7.8	7.8	49.5	2.0	14.4		

*) Lg=0.16 μm Wg=100 μm

The more the gate head shifts toward the source, the lower $C_{\rm gd}$. However, ΔX values less than -0.3 μm are, unfortunately, impractical, because the yield becomes worth little due to the accuracy of the alignment. Accordingly, ΔX of -0.2 μm is optimum where $C_{\rm gd}$ is reduced by 42 fF/mm and MSG is increased by 1 dB.

The equivalent circuit parameter extracted for the H-MESFET with ΔX of -0.2 μm is shown in Table I, where the gate width is 100 μm. The applied voltage was $V_{\rm gs} = 0.55$ V and $V_{\rm ds} = 1.5$ V. Although $C_{\rm gs}$ increases in 6.0 fF with the Au gate head shift, the increase is negligible compared with the magnitude of $C_{\rm gs}$. g_m and current gain cutoff frequency (fT) were unaffected by the Au gate head shift. Moreover, MSG and maximum oscillation frequency ($f_{\rm max}$) increase over the entire $V_{\rm gs}$ range.

IV. V-Band Amplifier

Fig. 2 shows the microphotograph of a fabricated V-band MMIC amplifier. The devices used for the amplifier have a gate length of 0.16 μm and a gate width of 50 μm, which consist of two gate fingers each with a 25-μm width. The Au gate heads of FET's were shifted 0.2 μm toward the source. The amplifier is composed of cascode-connected FET's with relatively long intermediate transmission lines of 300 μm to enhance an amplifier gain and bandwidth [7]. Coplanar waveguides were used for an effective compact layout [8]. The cascode line and input- and output-matching circuit consist of 50-Ω coplanar waveguides. The amplifier gain can be controlled at the gate voltage of the common-gate FET (V_c). The chip size is 0.95 mm $\times$ 0.85 mm.

Fig. 3 shows the S-parameters of the fabricated V-band MMIC amplifier. The bias condition is $V_d = 4.0$ V, $V_g = 0.5$ V, $V_c = 2.5$ V. The current consumption was 10 mA. The solid lines are the measured results and the broken are the simulated results using the HP-MDS. The measured and simulated results are in good agreement. The maximum gain achieved is as high as 9.7 dB at 55 GHz. A numerical simulation showed that if the Au gate head is placed at the center, the amplifier gain deteriorates by 0.7 dB due to the $C_{\rm gd}$ increase of 2.1 fF (42 fF/mm) in 50-μm FET. When the applied drain voltage fell to 3.5, 3.0, and 2.5 V, the amplifier gain decreased to

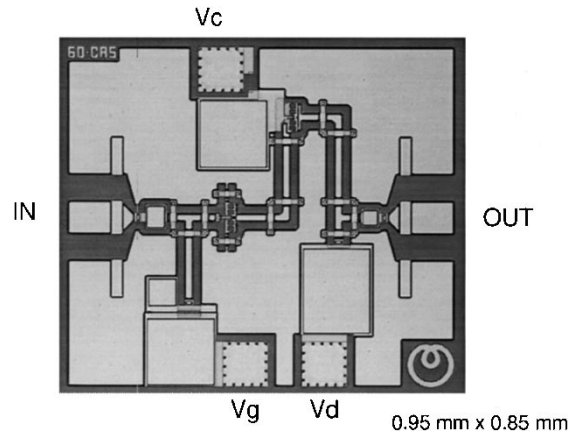

Fig. 2. Microphotograph of fabricated V-band MMIC amplifier by using cascode-connected FET's with relatively long cascode-connection line. Cascode line, and input- and output-matching circuit consist of 50-Ω coplanar waveguides.

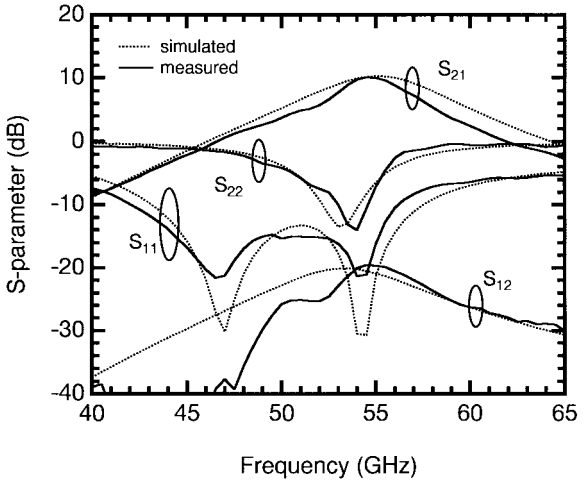

Fig. 3. Measured S-parameters of V-band MMIC amplifier. Applied voltages are $V_d = 4.0$ V, $V_g = 0.5$ V, and $V_c = 2.5$ V. Solid lines are measured results and broken are simulated ones.

8.8, 7.7, and 5.4 dB, respectively. From equivalent circuit parameter extraction of the H-MESFET's, $C_{\rm gd}$ decreases by 40 fF/mm per the increase of $V_{\rm ds}$ by 1 V. The decrease in the amplifier gain with lowered $V_{\rm ds}$ was mainly caused by the increase in the gate-to-drain capacitance. Hence, shifting the Au gate head by 0.2 μm toward the source is equivalent to increasing $V_{\rm ds}$ by 1 V in this amplifier. The noise figure of the MMIC amplifier is 6 dB at 55 GHz. This amplifier is preferable to gain applications. However, since the noise figure of the H-MESFET's is as low as 1.1 dB at 20 GHz, lower noise figure can be obtained if the input matching circuit is designed for optimum noise performance.

V. Conclusion

Self-aligned n^+ i-InGaP/n-InGaAs/i-GaAs H-MESFET's with a gate length of 0.16 μm were developed. The Au gate head was deliberately shifted 0.2 μm toward the source. This gate head shift decreased the gate-to-drain capacitance by 42 fF/mm and improved MSG at 10 GHz by 1 dB. Cascode-connected FET's constructed with an asymmetric gate heads yielded V-band MMIC amplifiers that offered a gain of 9.7 dB. H-MESFET's with asymmetric Au gate heads can be effectively applied for realizing highly integrated MMIC's in the millimeter-wave frequency range.

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